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MS-7502 uATX **Version: 1.1**

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - G33 North Bridge
Intel ICH9DH South Bridge

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LAN INTEL NINEVEH/EKRON
Audio Codec -- ALC888S
1394 Controller -- VT6308 (2-port)

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:


PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM:

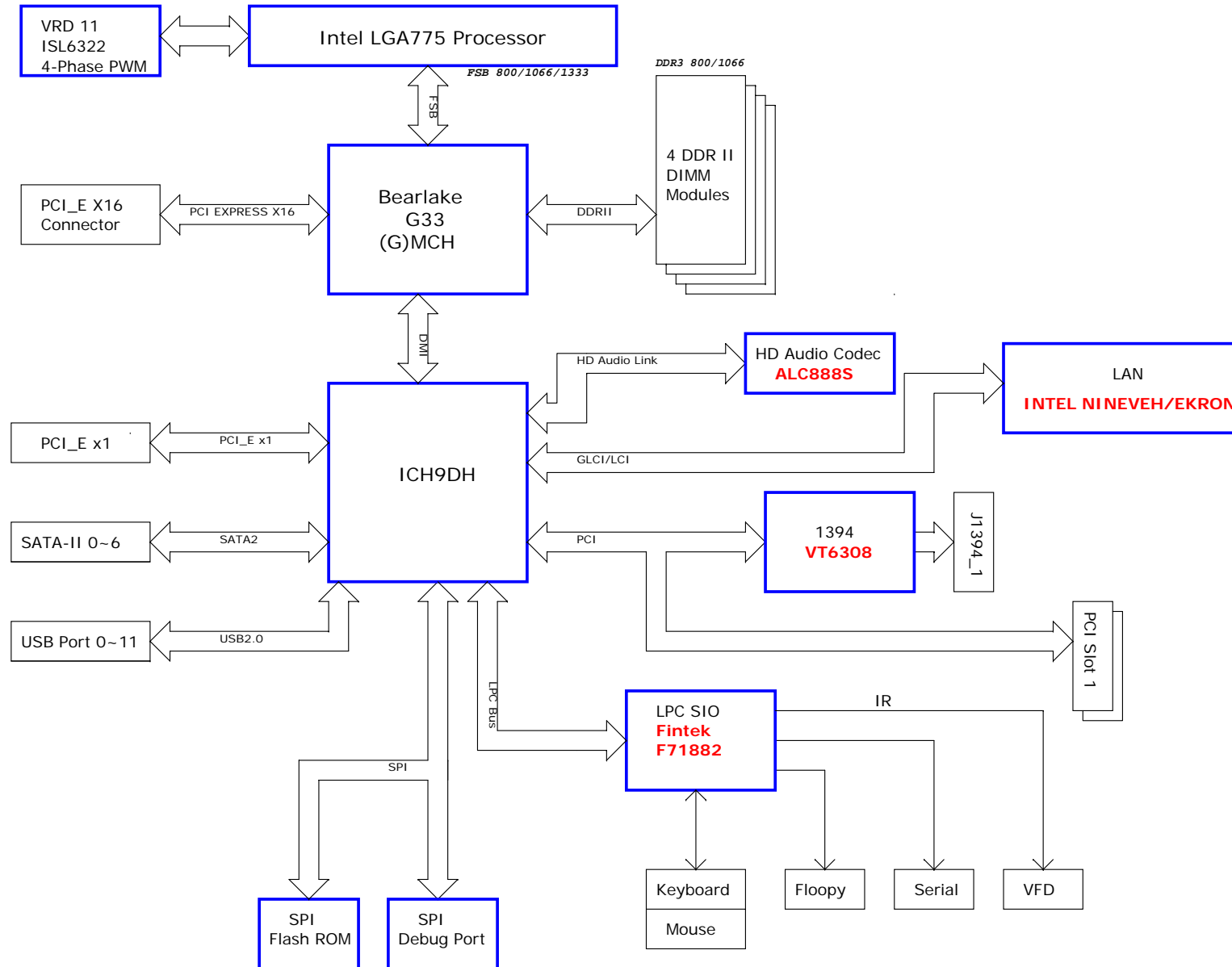
Intersil ISL6322 (4 Phases) w/ ISL6612 driver

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-P35/ICH9R	cfg-7502	
STD	Bearlake-G33/ICH9DH	cfg-7502	

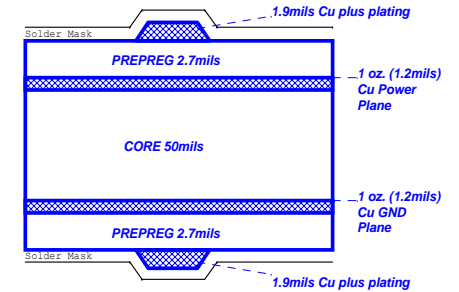
				MICRO-STAR INT'L CO.,LTD			
				MS-7502			
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Block Diagram



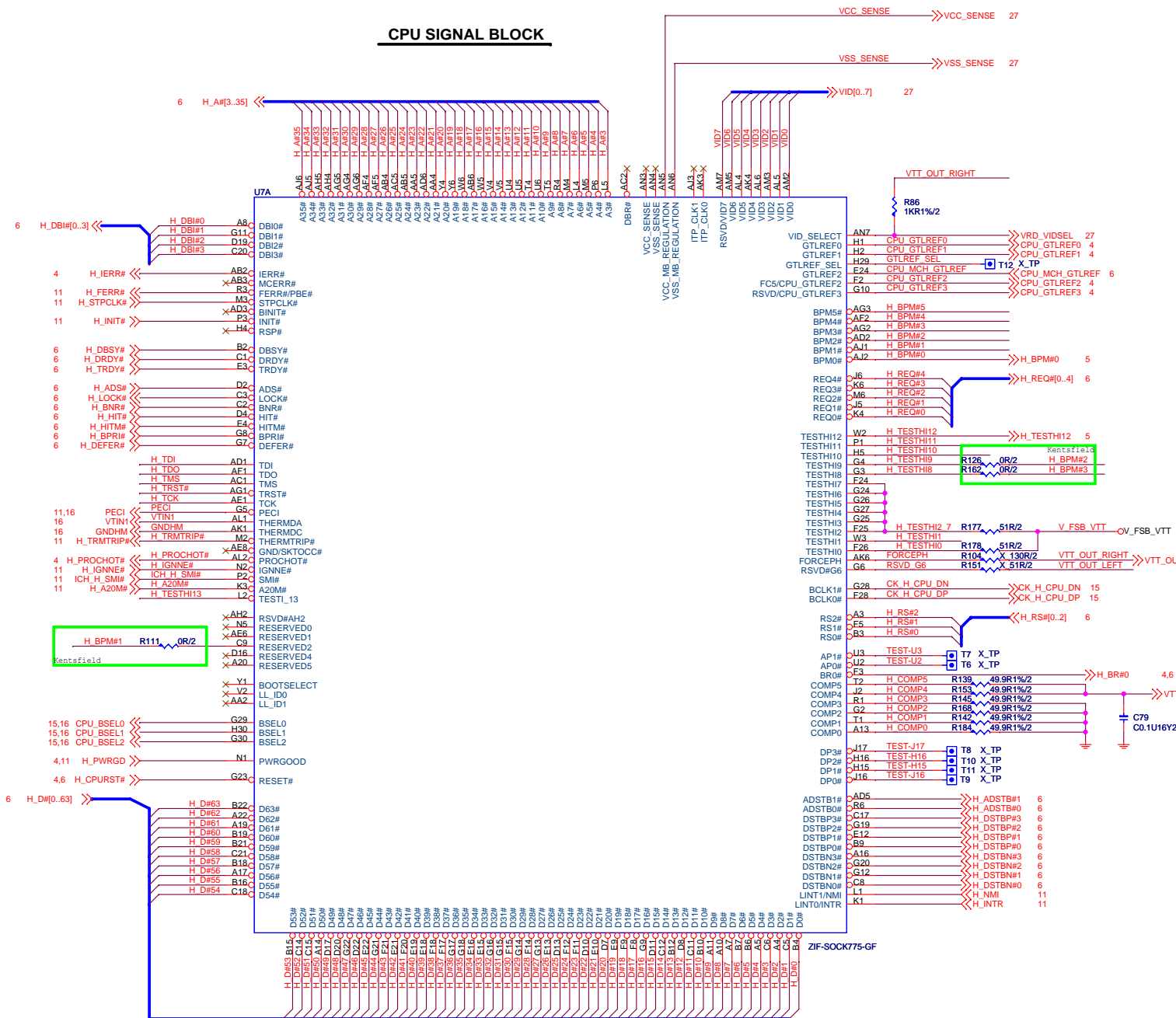
Board Stack-up

(1080 Prepreg Considerations)

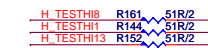
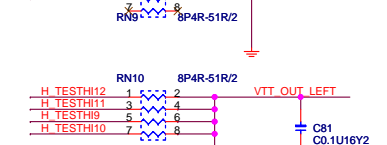
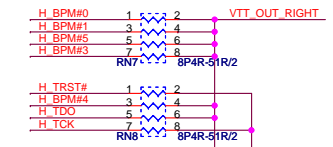
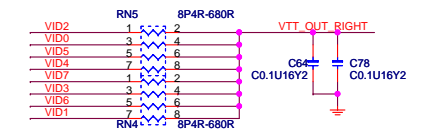


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

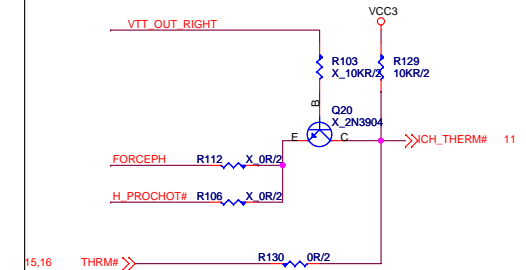
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



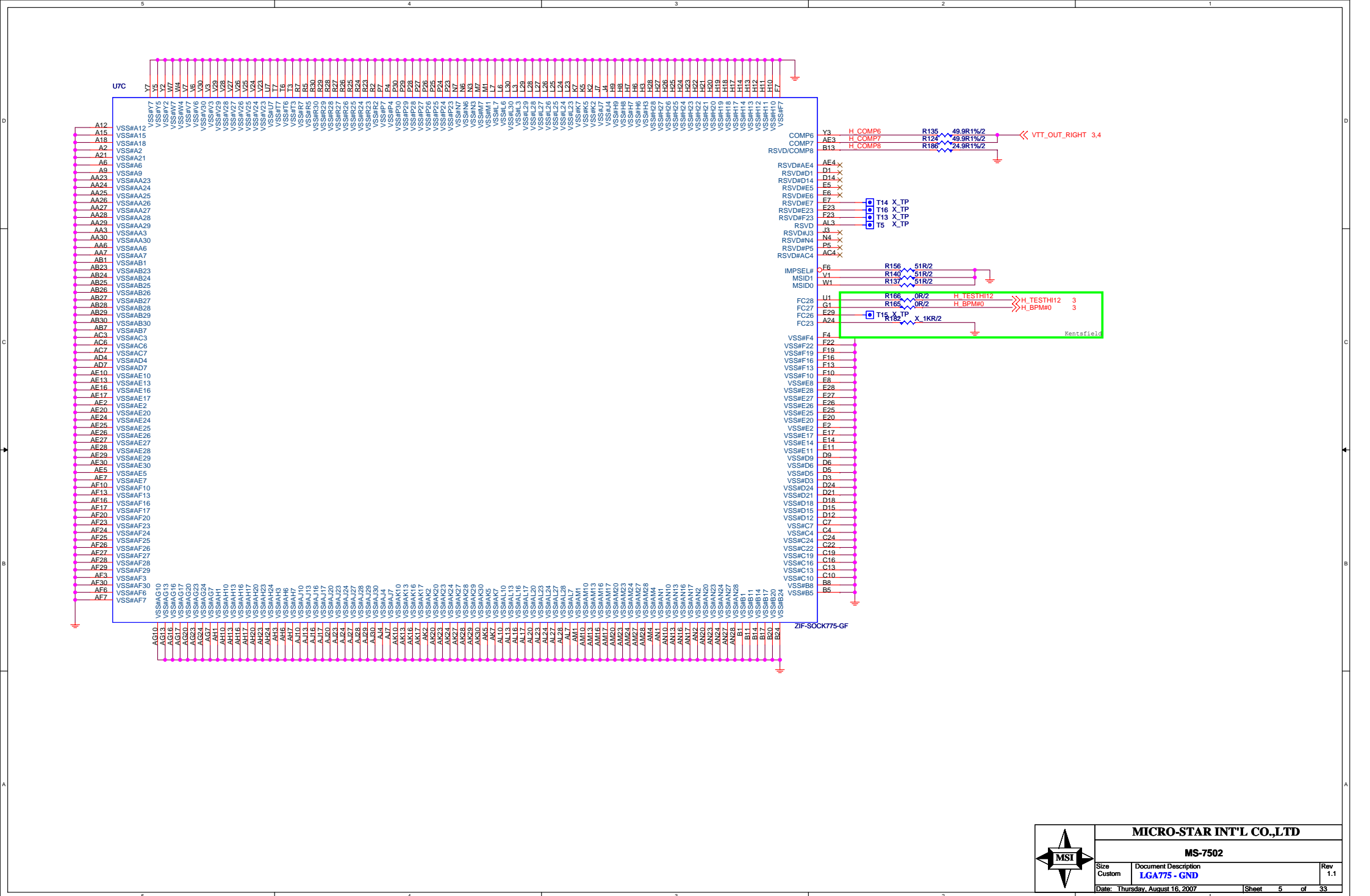
Thermal TRIP

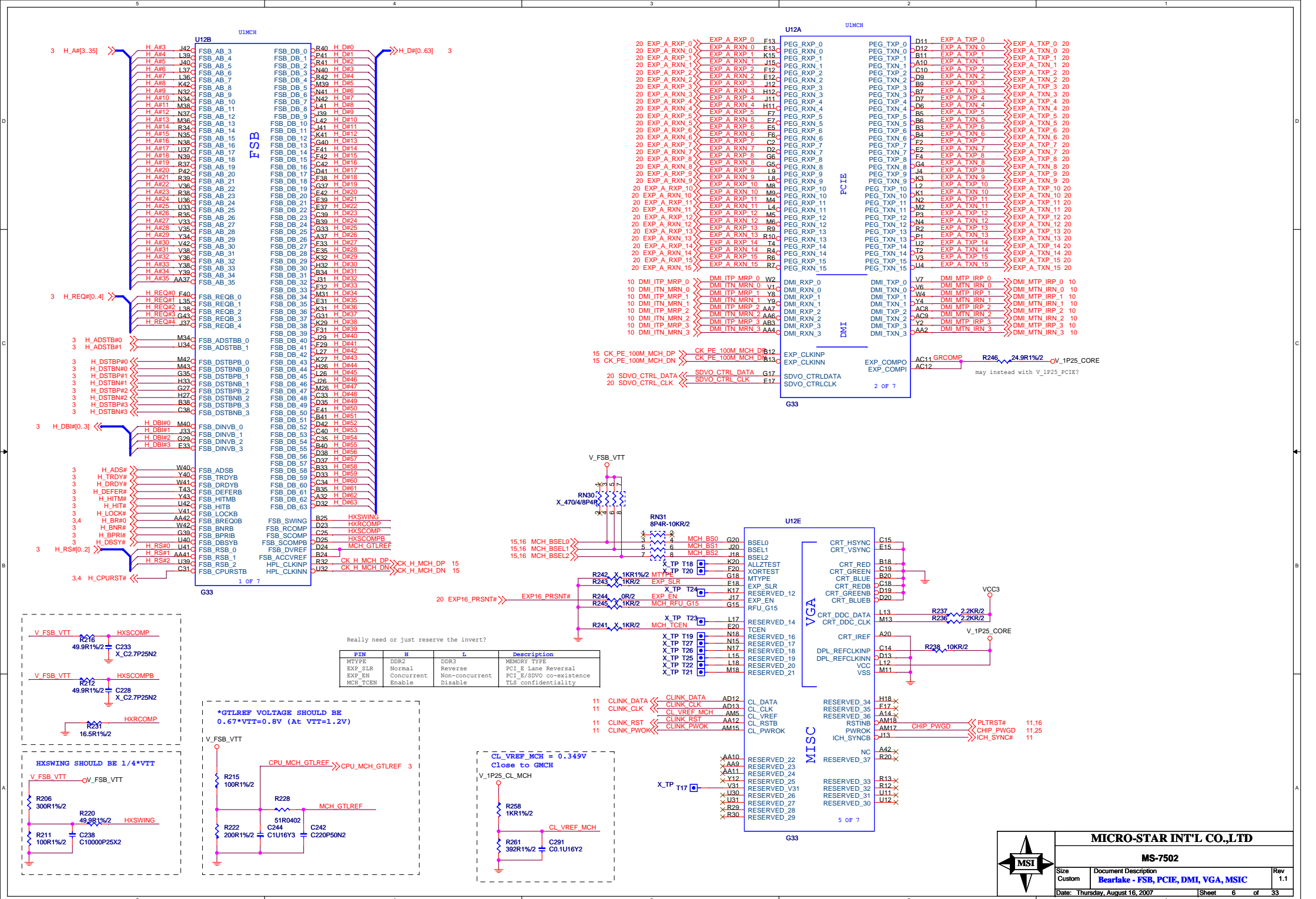


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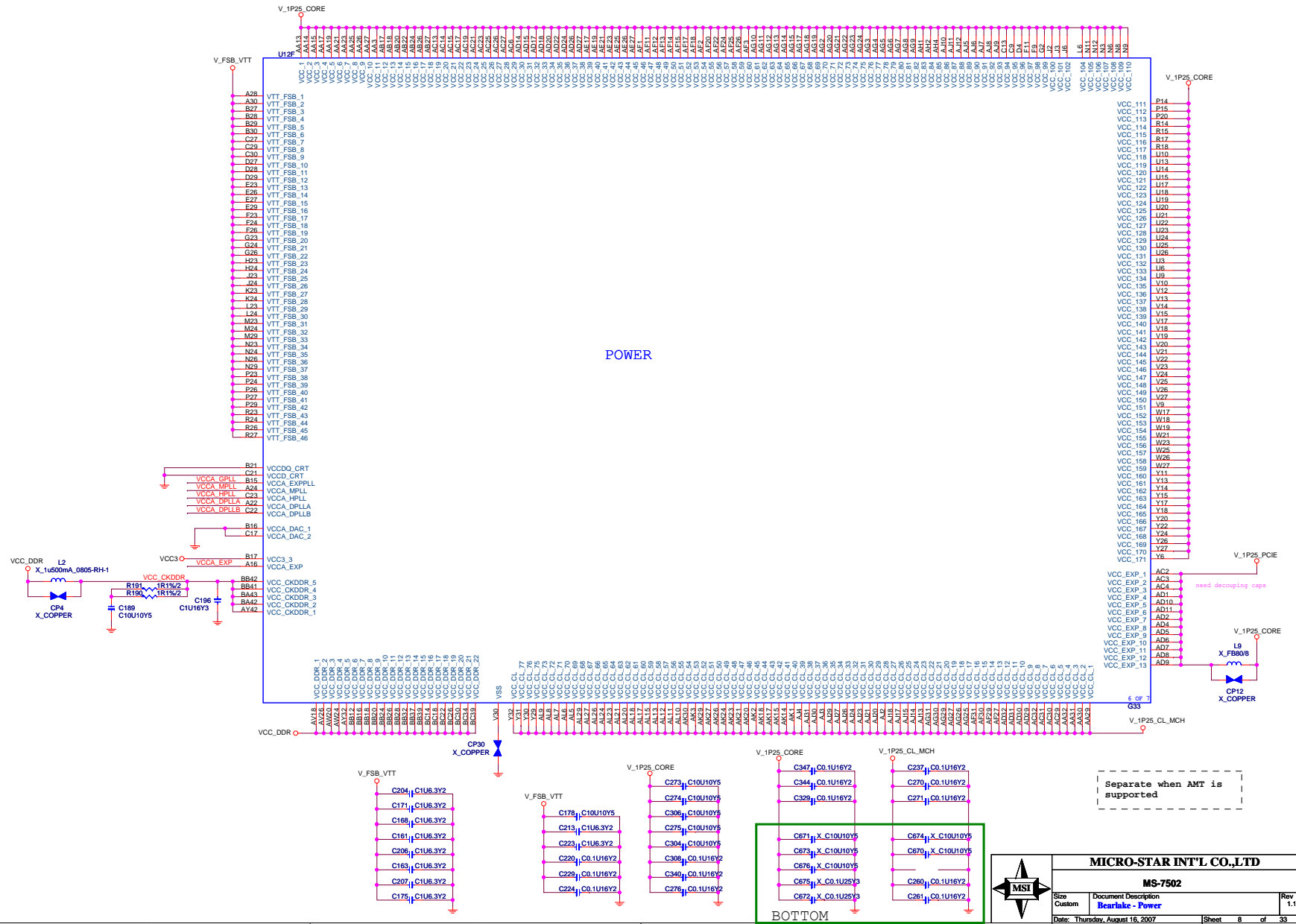
MICRO-STAR INT'L CO.,LTD

MS-7502

Size Custom	Document Description Bearlake - FSB, PCIE, DML, VGA, MSIC	Rev 1.1
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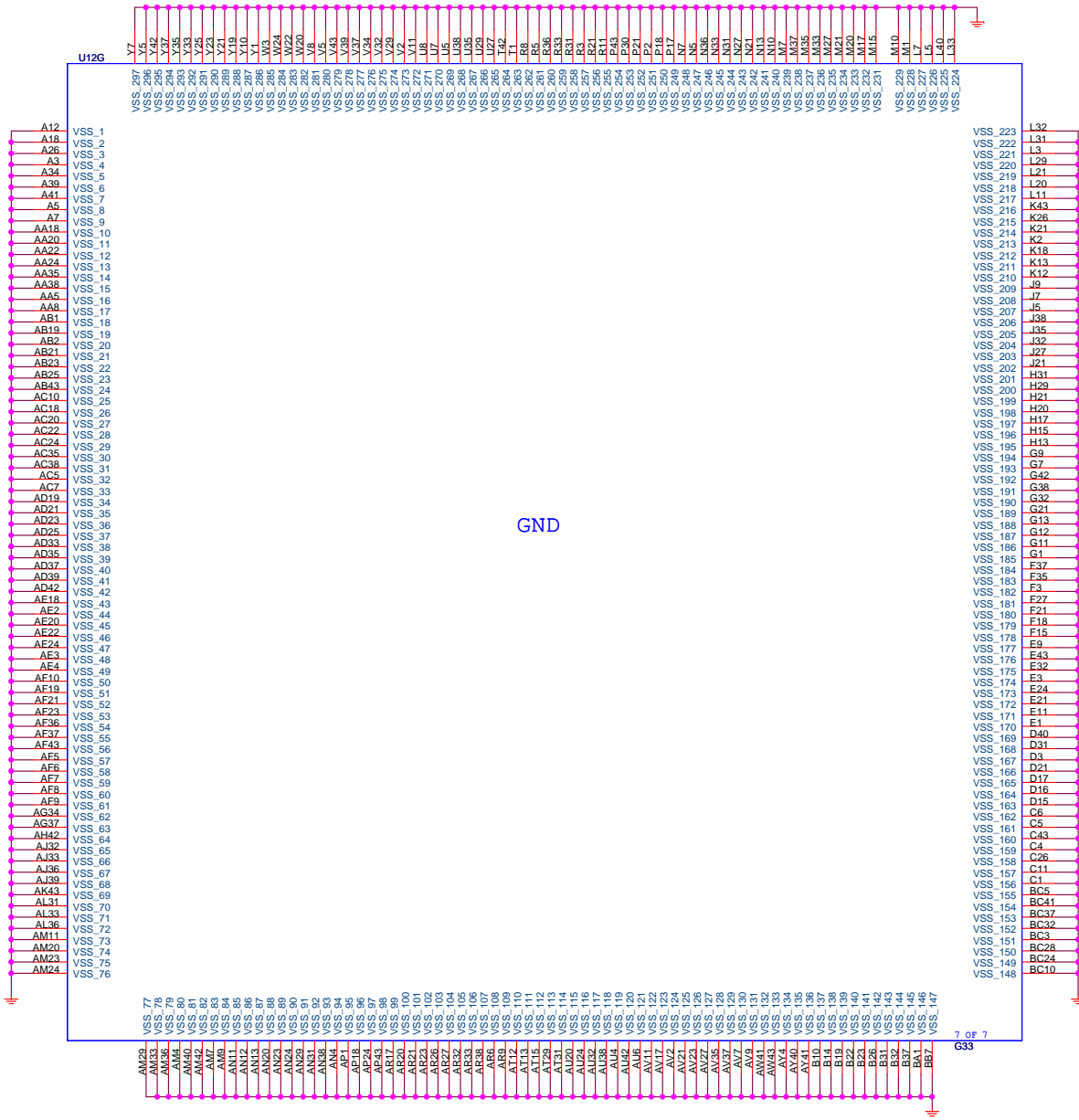
Figure 10 shows the schematic diagram of the power distribution network (PDN) for the L1000. The diagram illustrates the power flow from the input signals (V_1P25_CORE, V_1P25_CL_MCH, VCCA_EXP) through various components (inductors, capacitors, and resistors) to the output signals (VCCA_GPLL, VCCA_MPLL, VCCA_HPLL, VCCA_DPLL, VCCA_EXP). The components are labeled with their values and the manufacturer X_COPPER.

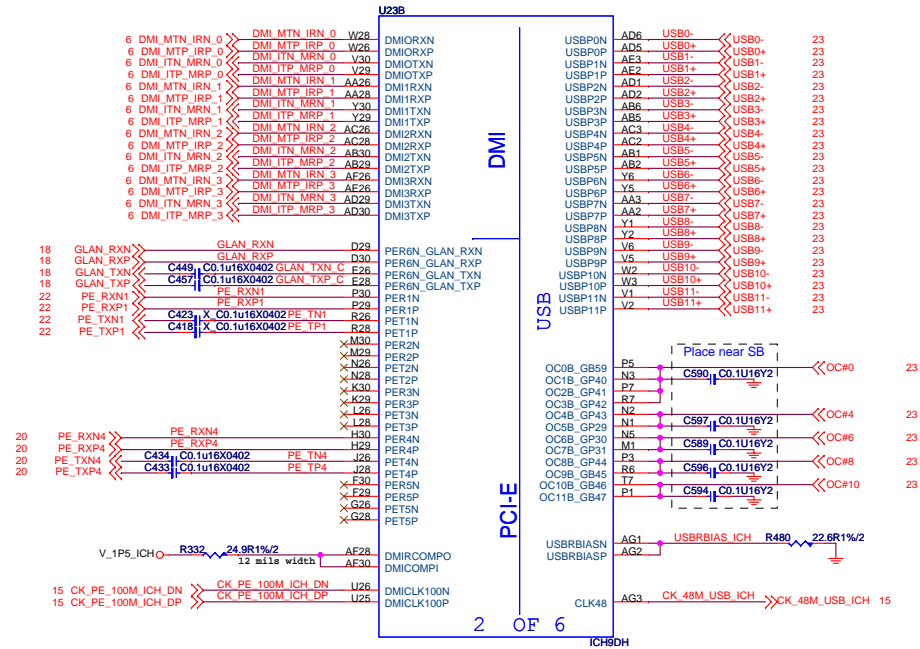
- Stage L1:** Input V_1P25_CORE, output VCCA_GPLL. Components: L8 (X_L10U_100mA_0805), R239 (1R1%/2), R240 (1R1%/2), C265 (X_C10U10Y5), C263 (C0.1U16Y2).
- Stage L2:** Input V_1P25_CL_MCH, output VCCA_MPLL. Components: L3 (X_L10U_100mA_0805), C6 (X_COPPER), R226 (1R1%/2), R225 (1R1%/2), C239 (C10U10Y5).
- Stage L3:** Input V_1P25_CL_MCH, output VCCA_HPLL. Components: L4 (X_L10U_100mA_0805), C7 (X_COPPER), C246 (C2.2U6.3Y3), C246 (C0.1U16Y2).
- Stage L4:** Input V_1P25_CORE, output VCCA_DPLL. Components: L5 (X_L10U_100mA_0805), C8 (X_COPPER), C249 (X_C10U10Y5), C250 (C0.1U16Y2).
- Stage L5:** Input V_1P25_CORE, output VCCA_DPLL. Components: L6 (X_L10U_100mA_0805), C9 (X_COPPER), C255 (X_C10U10Y5), C254 (C0.1U16Y2).
- Stage L7:** Input VCCA_EXP, output VCCA_EXP. Components: L7 (L0.1U_50mA), C262 (X_C10U10Y5), C259 (C0.1U16Y2).



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R474 1KR1%/2 PGNT#0
R387 X 1KR/2 SPI_CS1#

BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CSI#
FWH	1	1
SPI	0	1
PCI	1	0

PGNT#[3:0] Internal Pull-up



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

```
HDA_SDOUT/HDA_SYNC strap PCI_E port
configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X          11:0X/0X/4X
```



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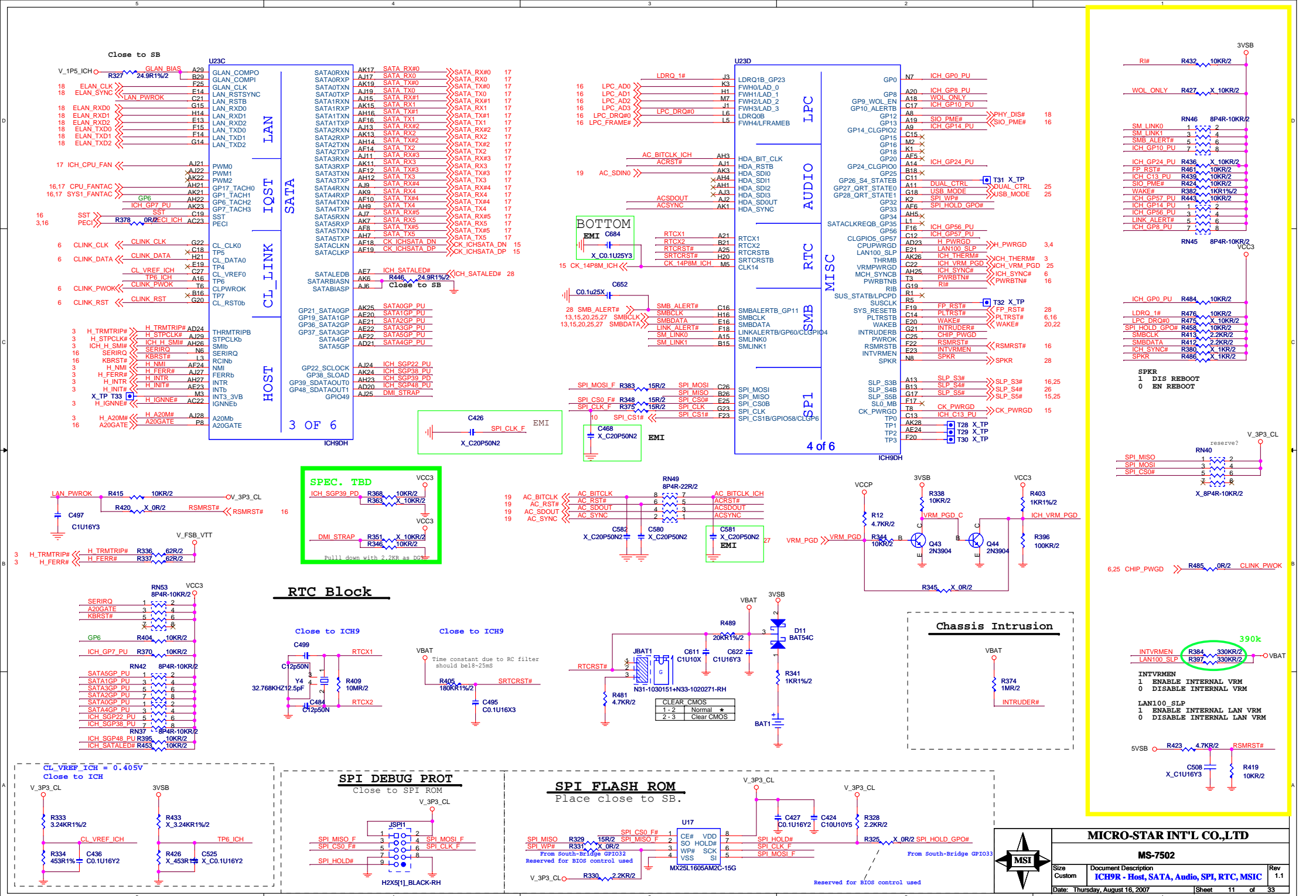
MS-7502

Size	Document Description
Custom	ICH9R - PCI, DMI, USB, PCIE & Slots

Rev	1.1
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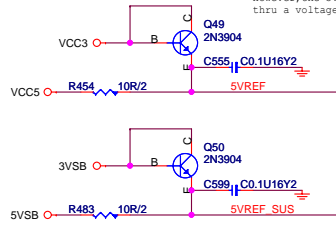
Date: Thursday, August 16, 2007

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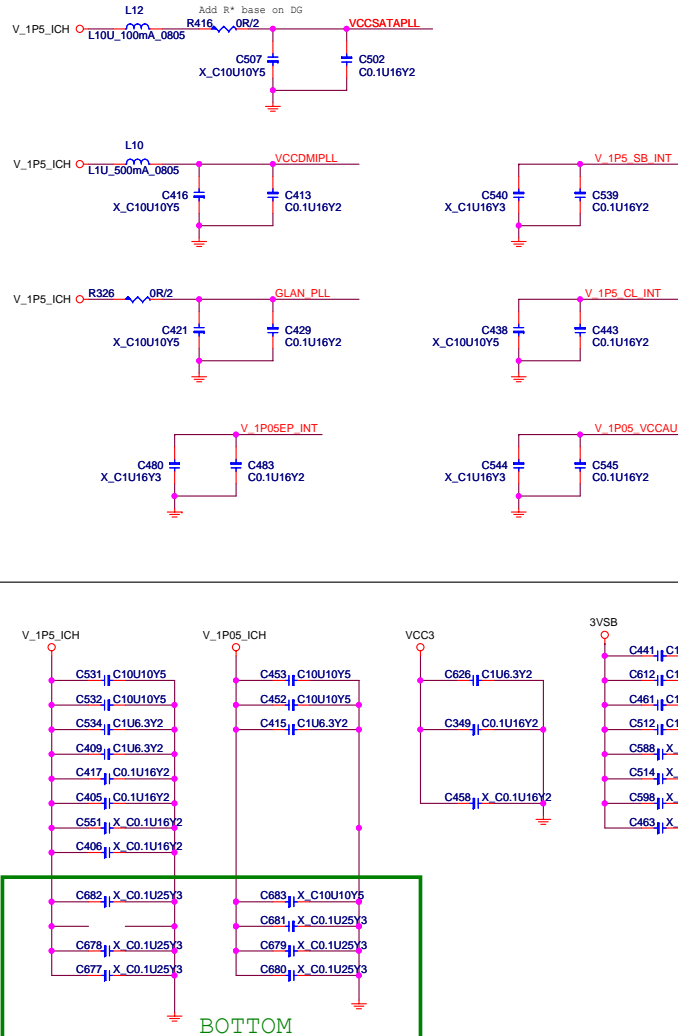


5VREF & 5VREF_SUS Sequencing Circuit

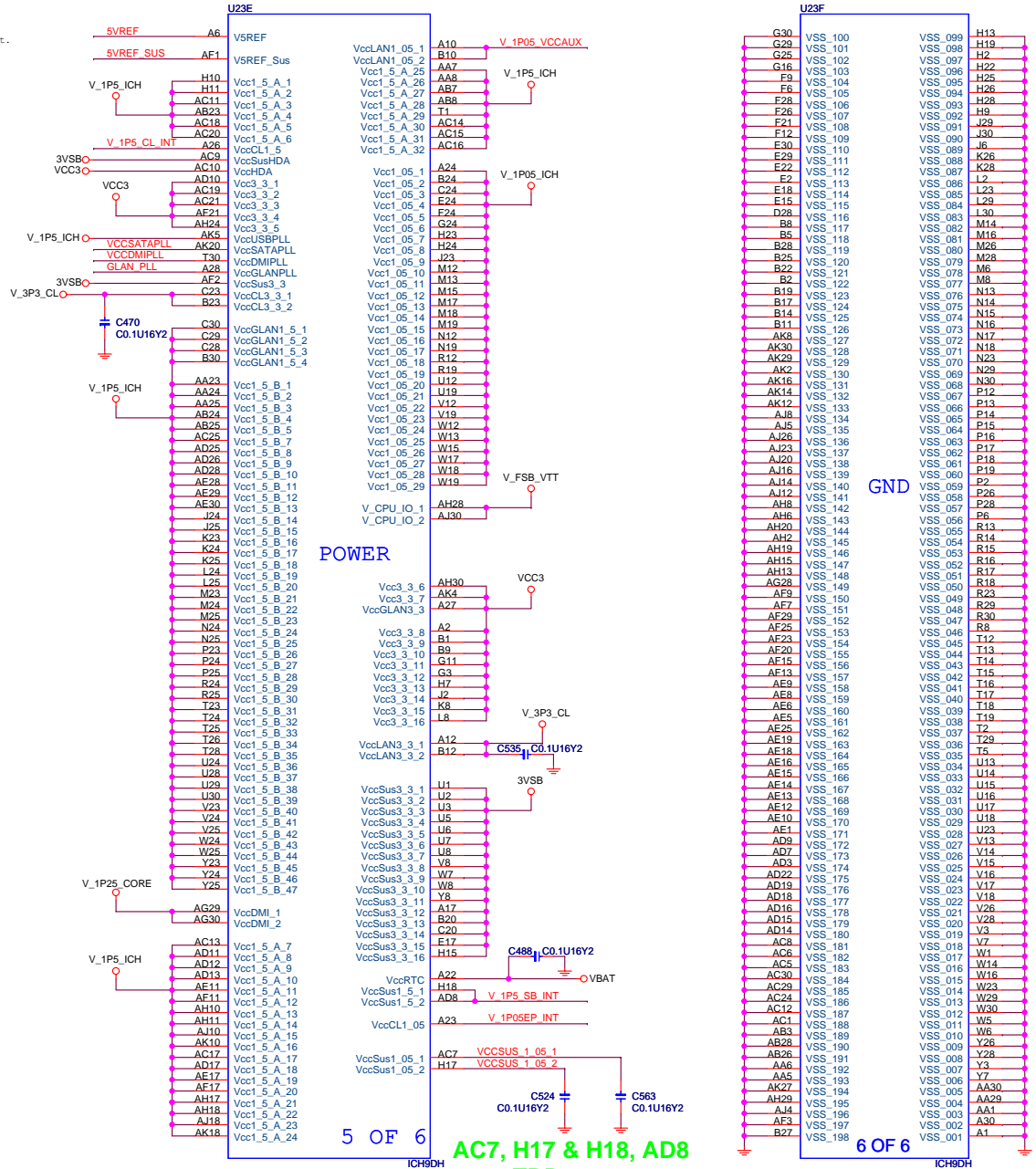
V5REF must be powered up before VCC3 or after VCC3 within 0.7V.
Also, V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



SB POWER



BOTTOM



POWER

5 OF 6

AC7, H17 & H18, AD8
spec TBD

GND

6 OF 6



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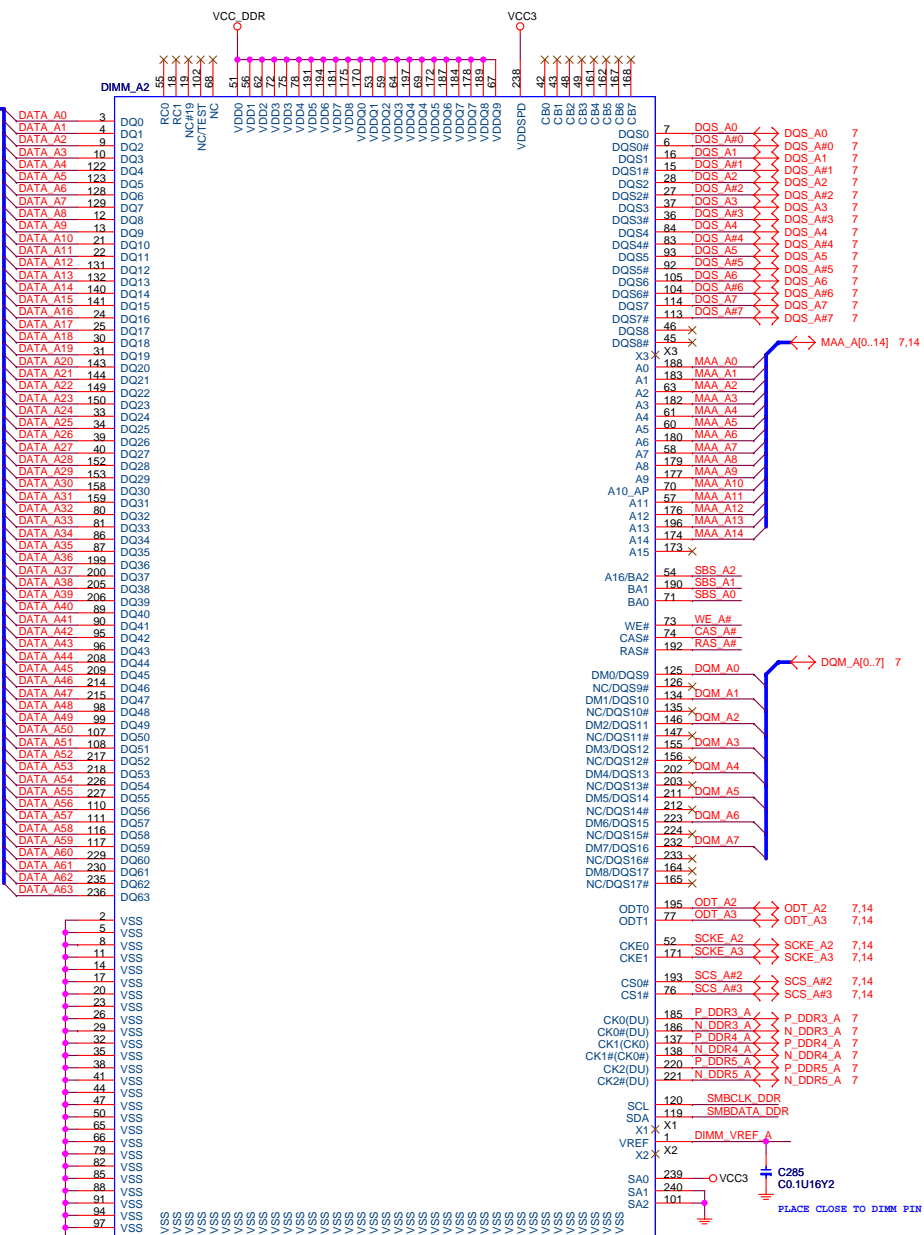
DDRII DIMM_A1



ADDRESS: 000
0xA0

SMBCLK_DDR R74 33R/2
SMBDATA_DDR R78 33R/2

DDRII DIMM_A2



ADDRESS: 001
0xA2

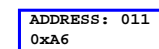
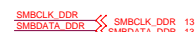
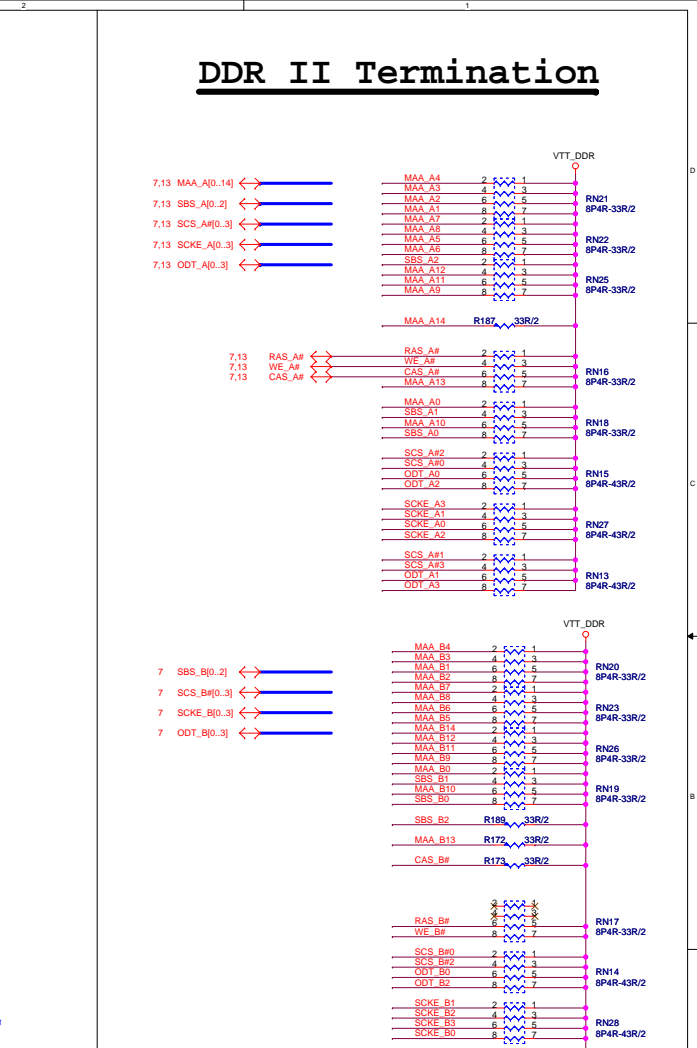
SMBCLK_DDR R74 33R/2
SMBDATA_DDR R78 33R/2



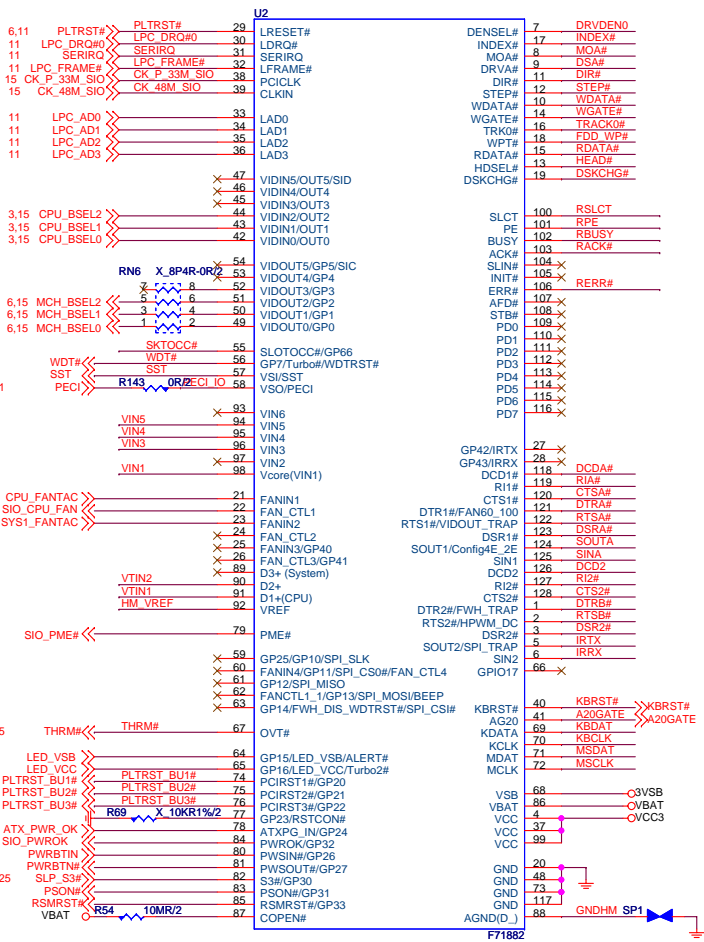
MICRO-STAR INT'L CO.,LTD

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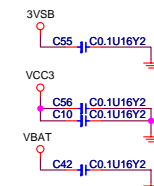
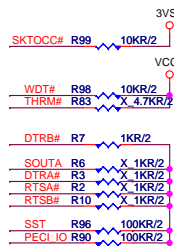
Size	Document Description	Rev
Custom	DDR2 CHANNEL-A	1.1
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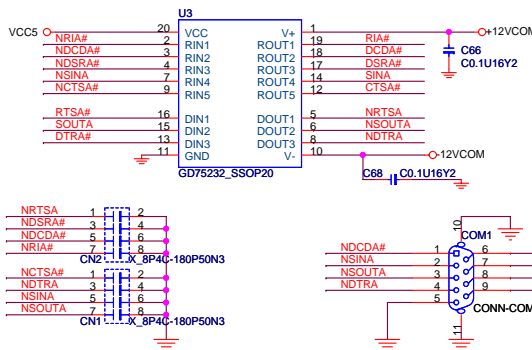
MICRO-STAR INT'L CO.,LTD			
MS-7502			
Size Custom	Document Description DDR2 CHANNEL-B/DDR II Termination		Rev 1.1
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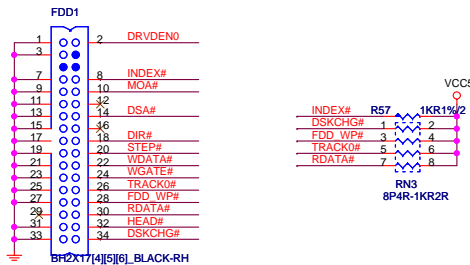
LPC I/O STRAPPING RESISTOR

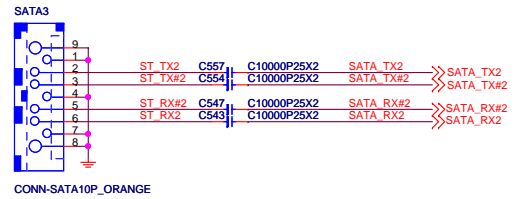
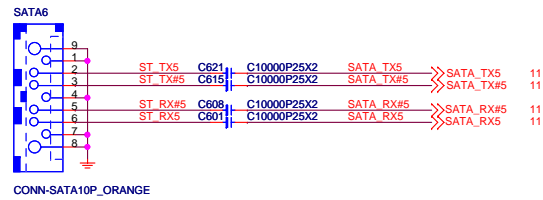
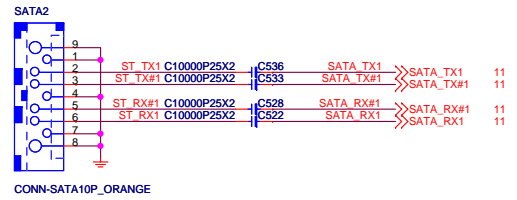
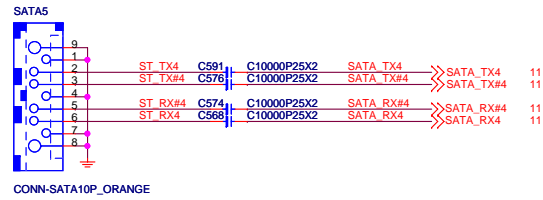
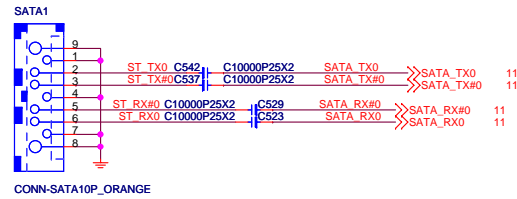
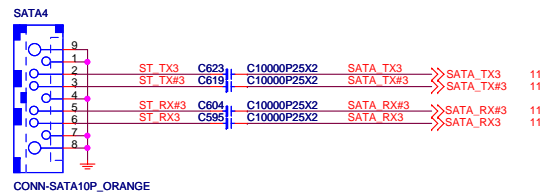


SERIAL PORT 1

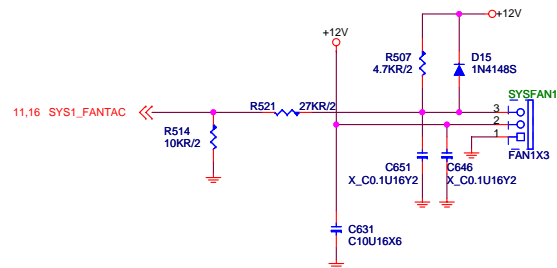
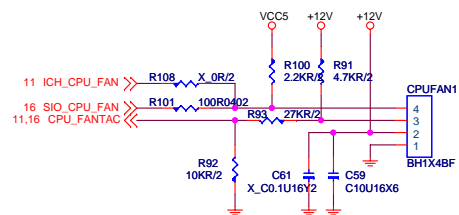


FLOPPY CONNECTOR





FAN-COUNTROL CIRCUIT



Modify System FAN circuit & Remove PWR_FAN
for spec need 3pin DC Smart FAN 07.3.30 by Robile

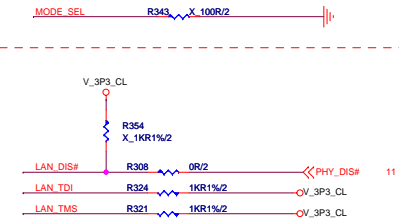


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LAN CONNECTOR



Place close to LAN chip



V_{3P3_CL}

R342 X_1R1206

R353 X_1R1206

Q47 X_P-BCP69_SOT223

LAN_V_PbG

EC42

X_ELC470U10V180mA

C685

C420

C460

C471

C503

C435

C432 X_C01U16V2

X_C10U6.3X5

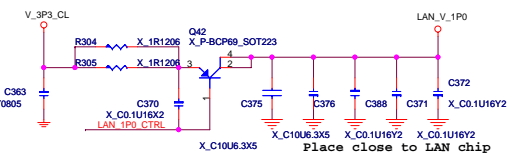
X_C10U6.3X5

X_C10U16V2

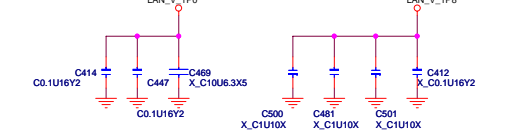
X_C10U16V2

Place close to LAN chip

YELLOW : For Active/Link



IAN V 1D0 IAN V 1D0

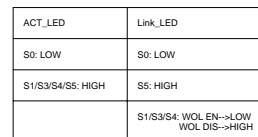




Stuff For EKRON
Empty for NINEVEH



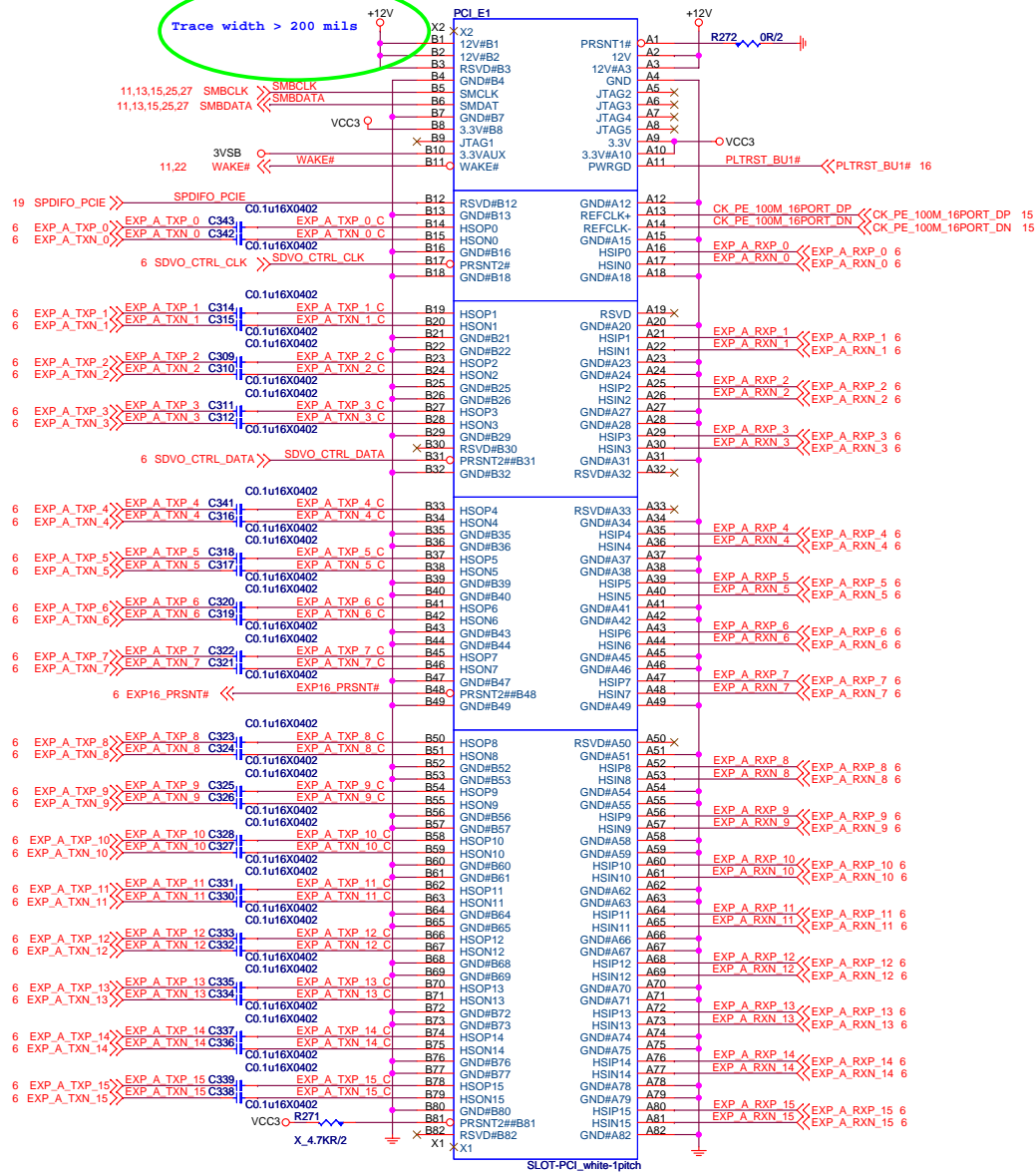
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Size C	Document Description INTEL NINEVEH/EKRON	Rev 1.1
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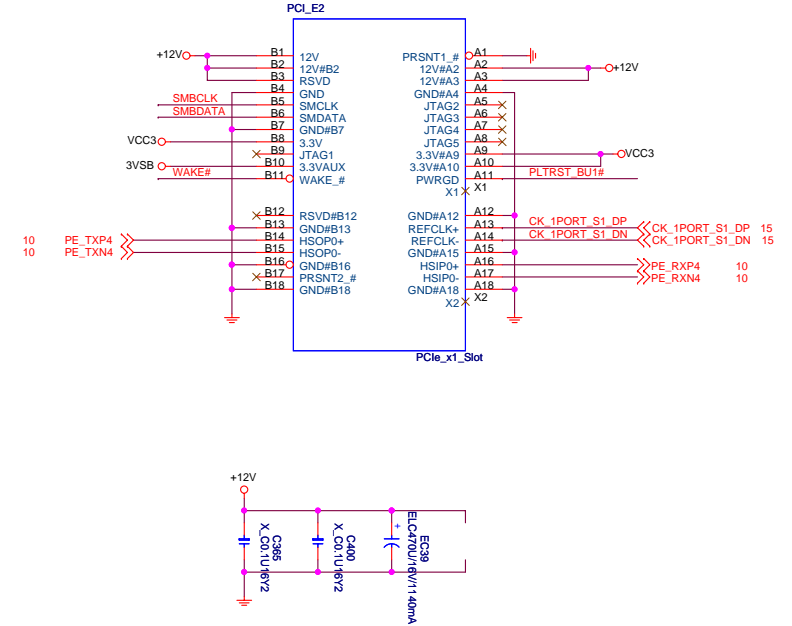


Giga-Lan		10/100-Lan	
N58-22F0181-842		N58-22F0061-842 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

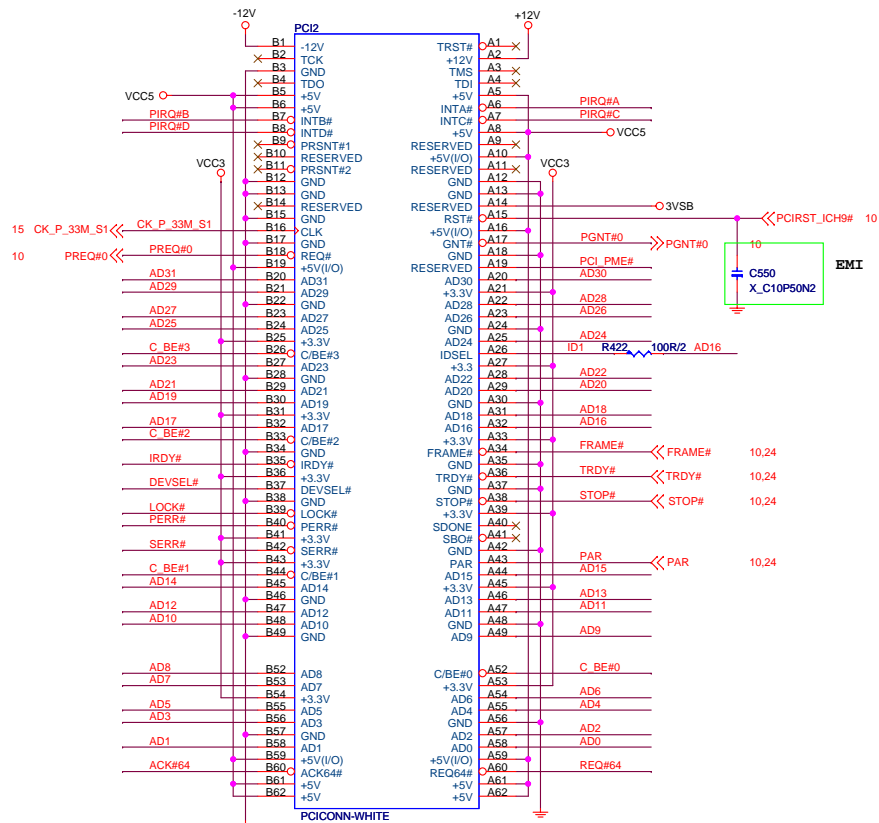
PCI_Express X16 Slot



PCI_Express X4 Slot (Share with PCI_E x1 Slots)



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD16

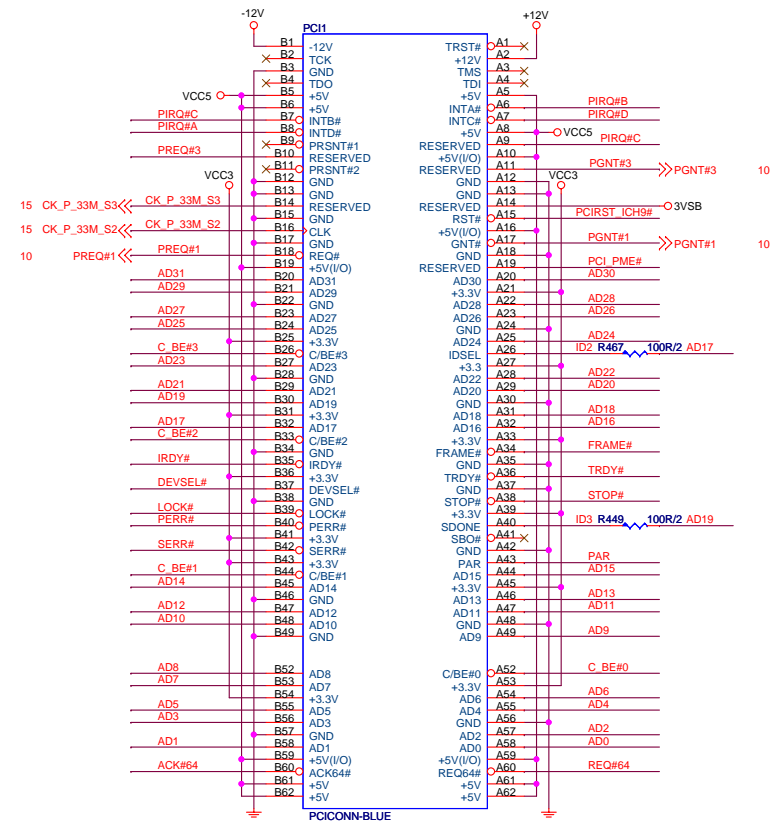
MASTER = PREQ#0

PIRQ#A

10.24 AD[31..0] << AD[31..0]

10.24 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD17

MASTER = PREQ#1

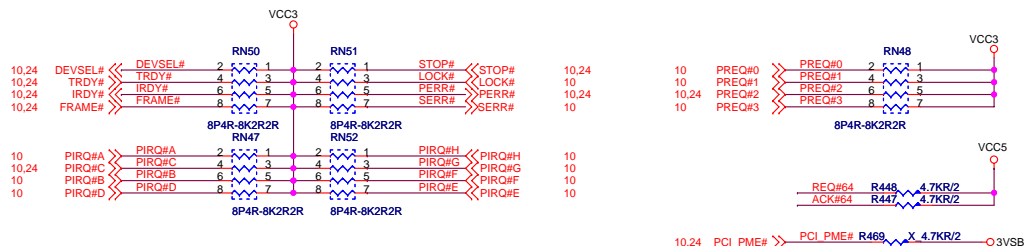
PIRQ#B

IDSEL = AD19

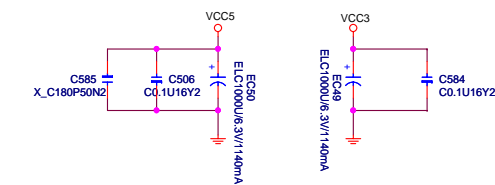
MASTER = PREQ#3

PIRQ#C

PCI PULL-UP / DOWN RESISTORS



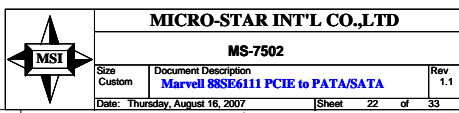
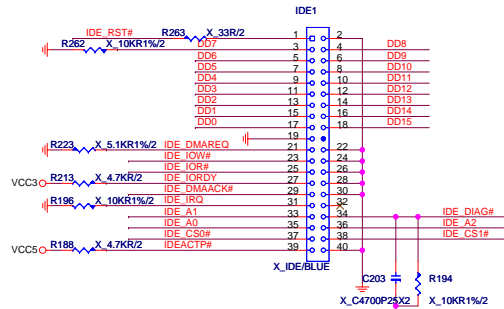
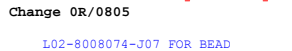
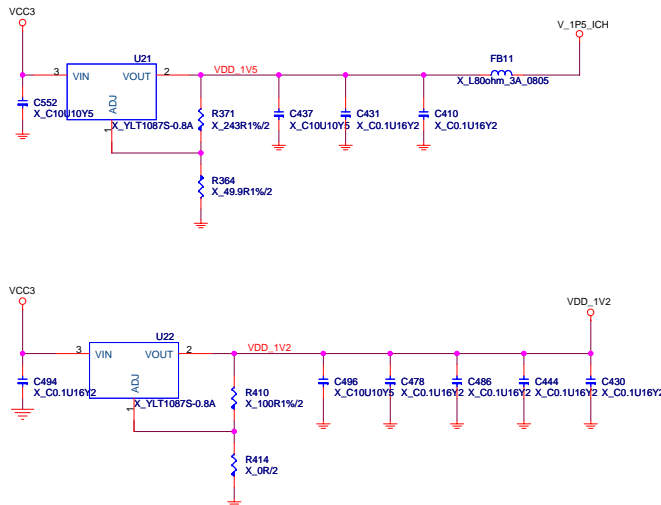
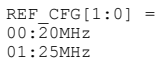
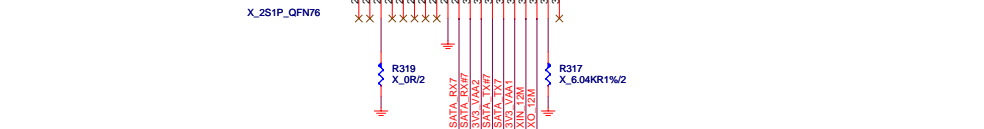
PCI SLOT DECOUPLING CAPACITORS



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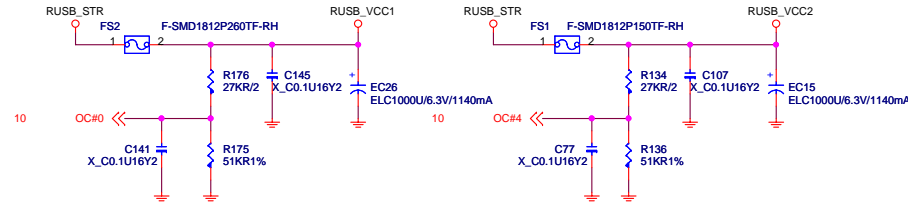
Rear USB Connector

USB POWER FOR PORT 0,1,2,3

NEAR CONNECTOR

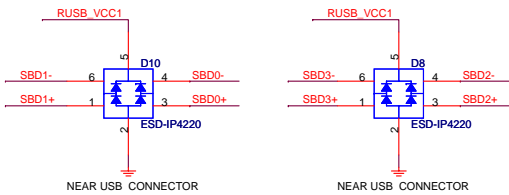
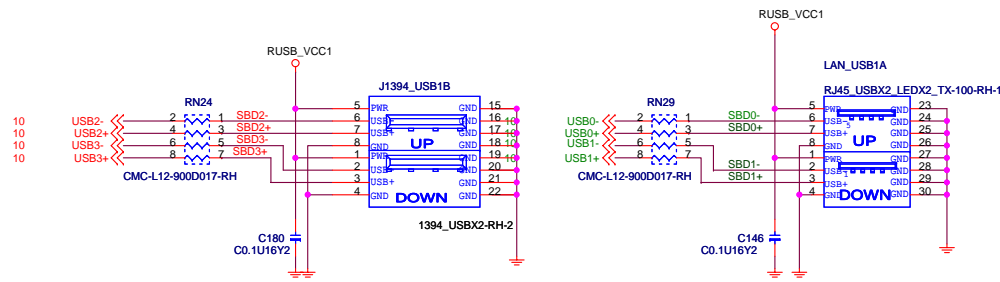
USB POWER FOR PORT 4,5

NEAR CONNECTOR

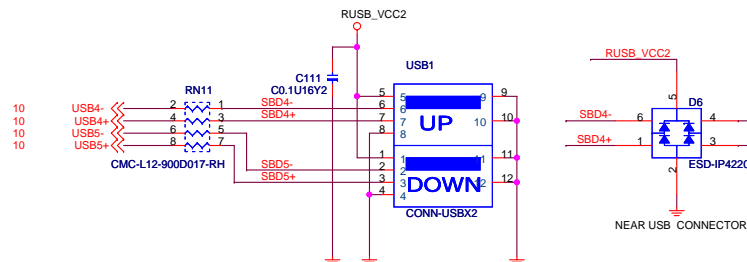


REAR USB PORT 2,3(With 1394)

REAR USB PORT 0,1 (With LAN)



REAR USB PORT 4,5



Front USB Connector

USB POWER FOR PORT 6,7

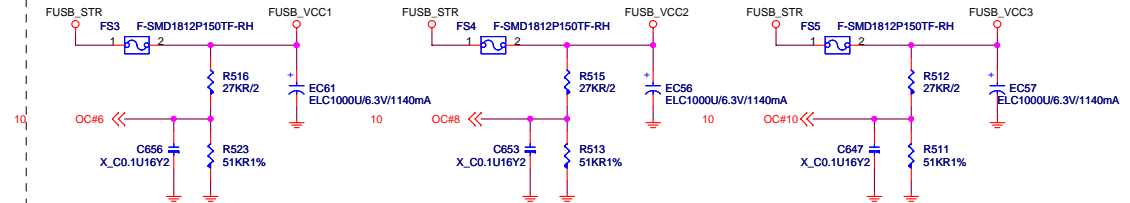
NEAR CONNECTOR

USB POWER FOR PORT 8,9

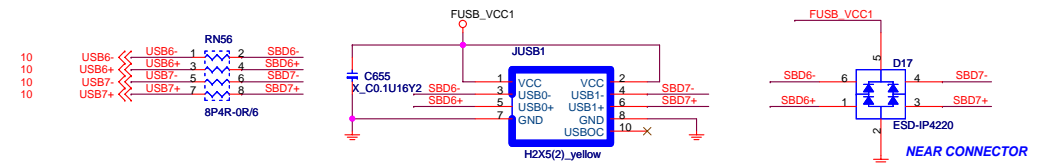
NEAR CONNECTOR

USB POWER FOR PORT 10,11

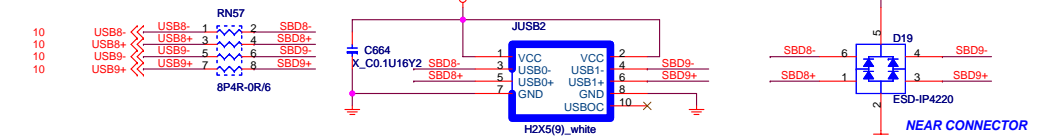
NEAR CONNECTOR



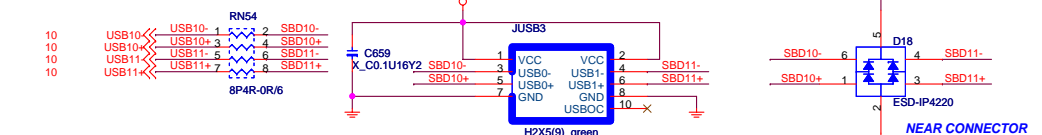
FRONT USB PORT 6,7



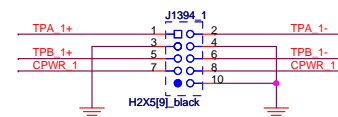
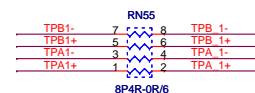
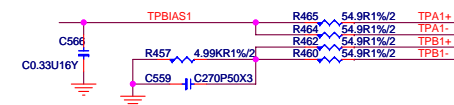
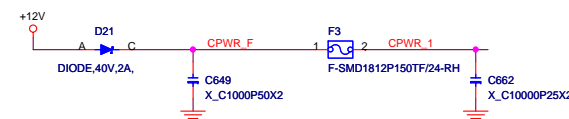
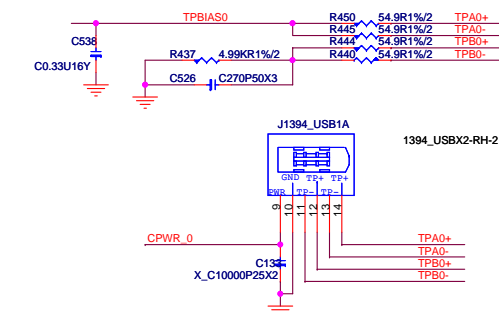
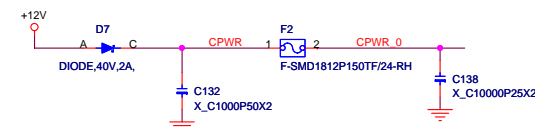
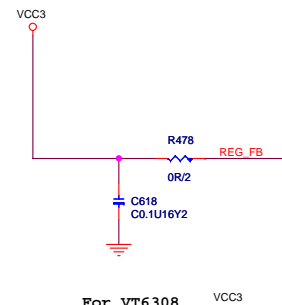
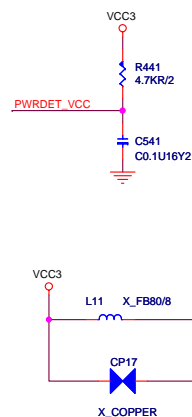
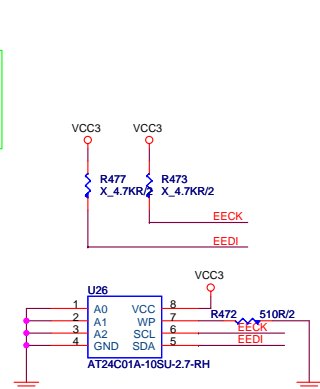
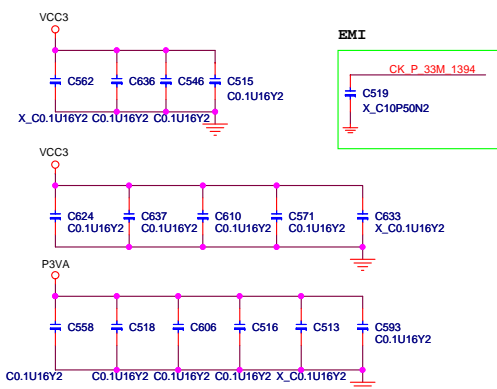
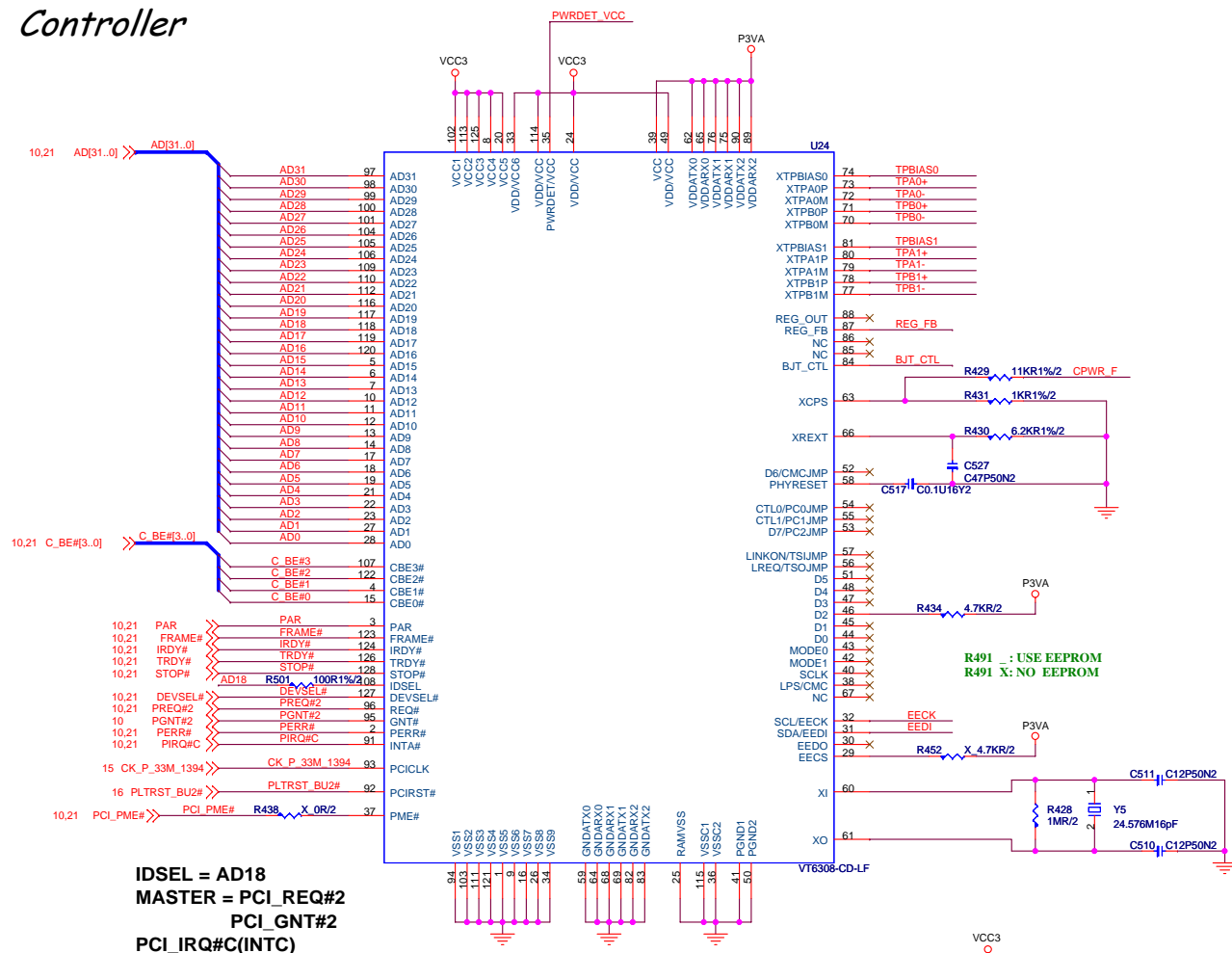
FRONT USB PORT 8,9



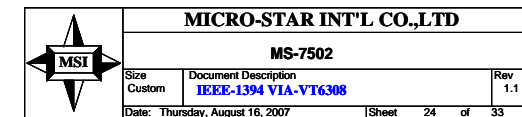
FRONT USB PORT 10,11



1394a OHCI Link Layer Controller



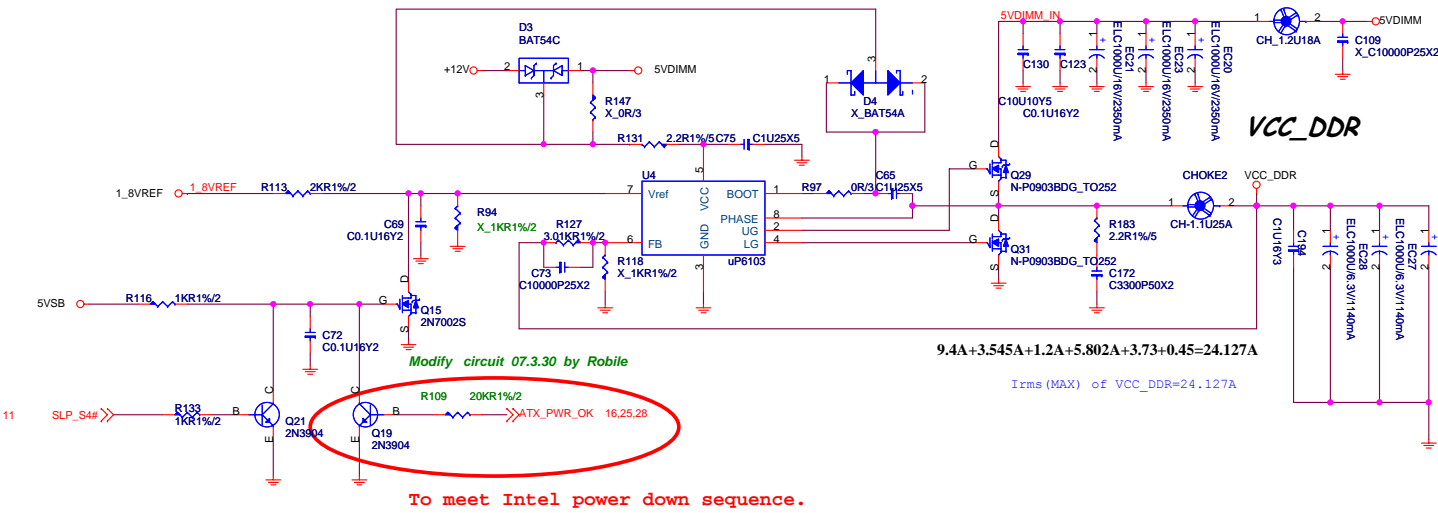
For Intel 1394 pinheader



DDR II 1.8V POWER

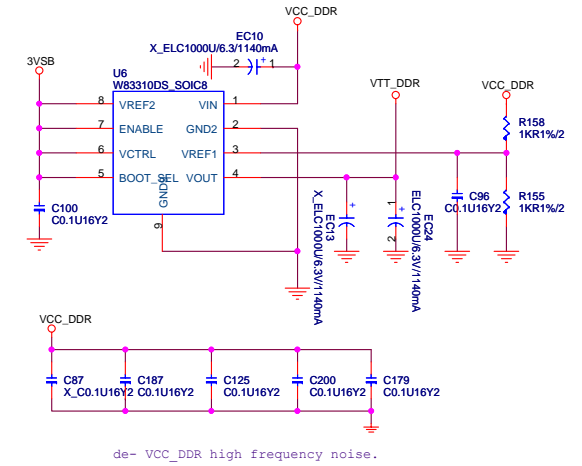
$$\text{Irripple} = 24.127 \times 0.8 \times \sqrt{(1.8/5)} \times \sqrt{(1-1.8/5)} / 1 = 9.264768\text{A}$$

$$2.35 \times 3 \times 1.7 = 11.985\text{A} > 9.264768\text{A}$$



DDR VTT Power

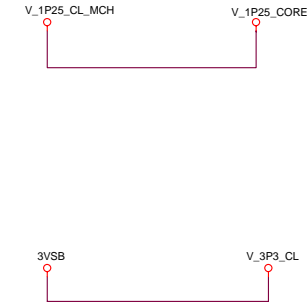
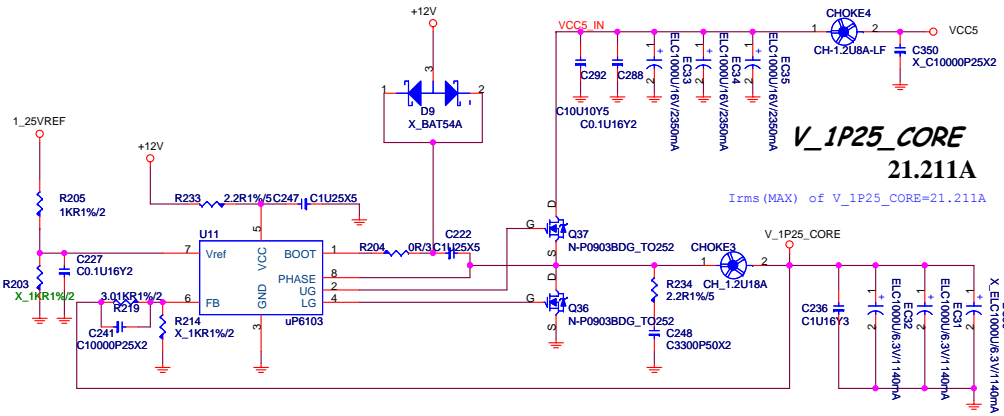
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



NB 1.25V POWER

$$\text{Irripple} = 21.211 \times 0.8 \times \sqrt{(1.25/5)} \times \sqrt{(1-1.25/5)} / 1 = 7.347706\text{A}$$

$$2.35 \times 3 \times 1.7 = 11.985\text{A} > 7.347706\text{A}$$

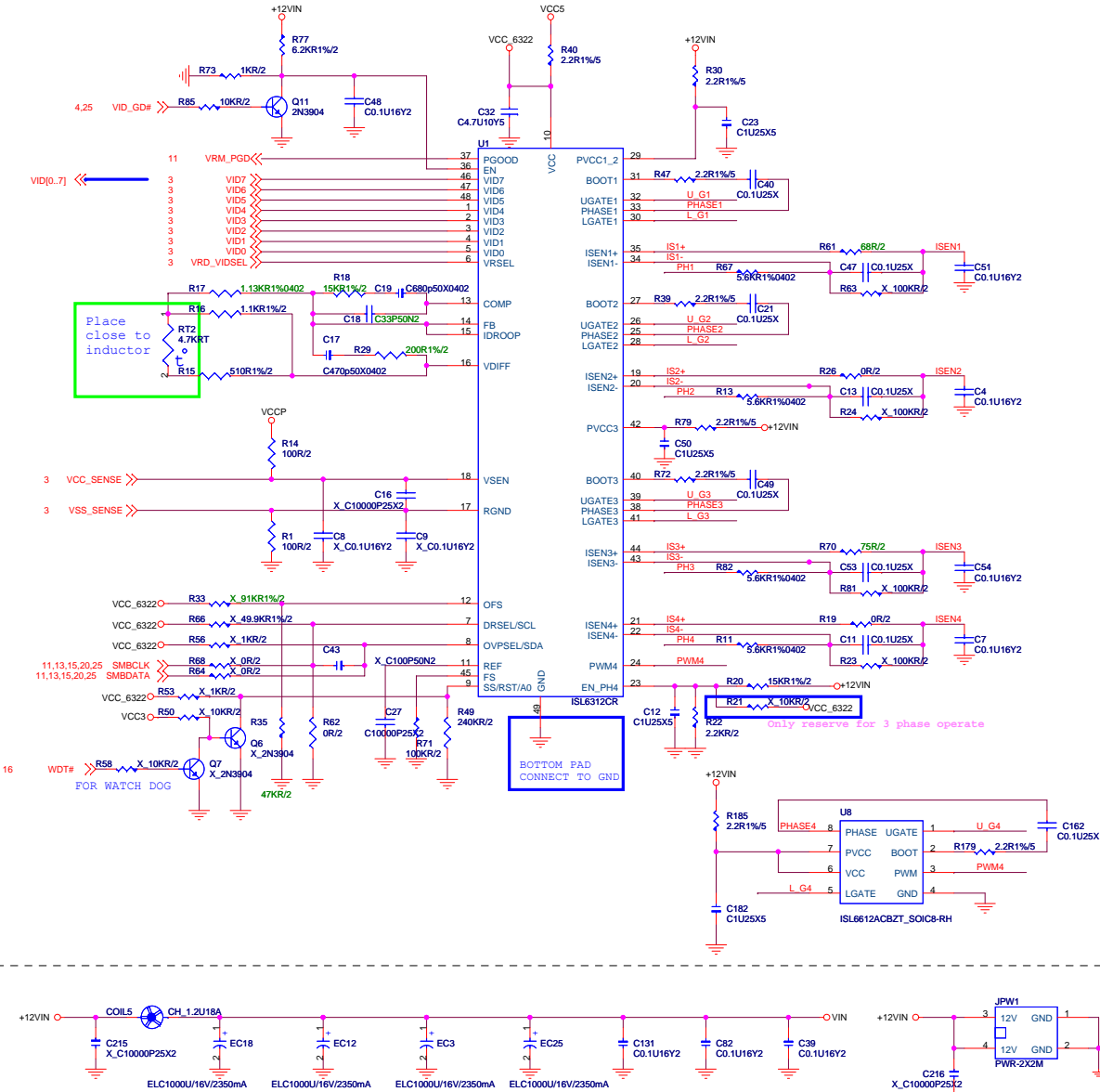


MICRO-STAR INT'L CO.,LTD

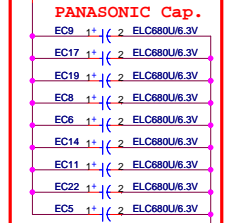
MS-7502

Size	Document Description	Rev
Custom	NB Core Power & DDR Power	1.1
Date: Thursday, August 16, 2007	Sheet 26 of 33	

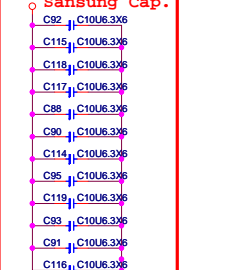
Voltage Regular Module



680uF EL Capacitors



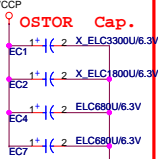
MLCC Inside Socket



SP Capacitors

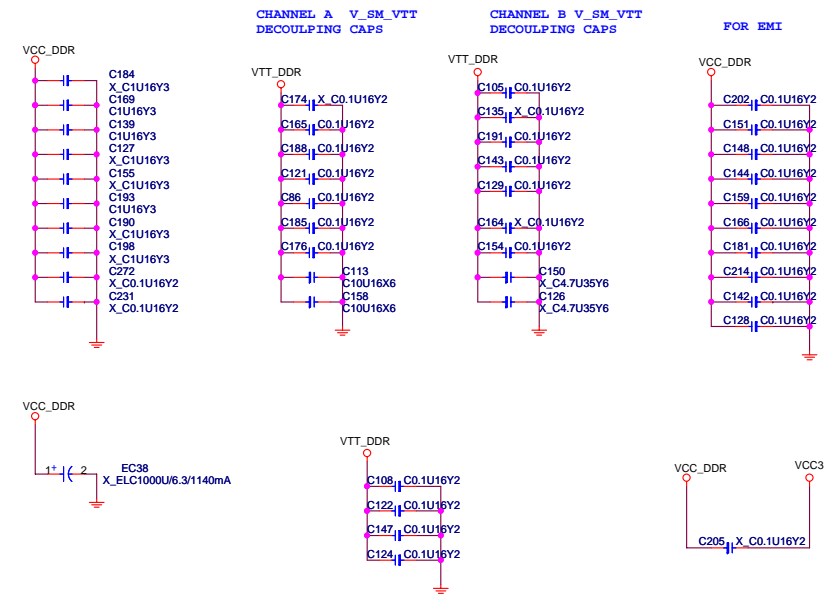
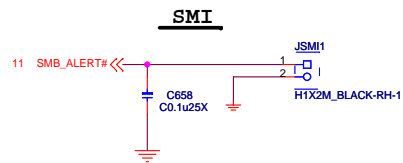
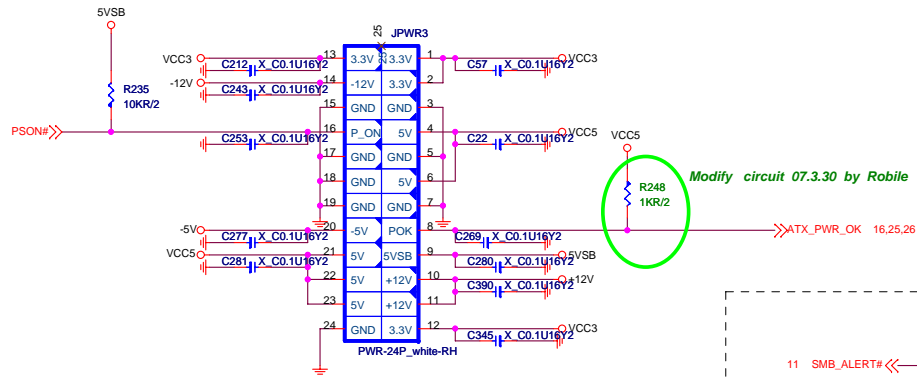


EL Capacitors

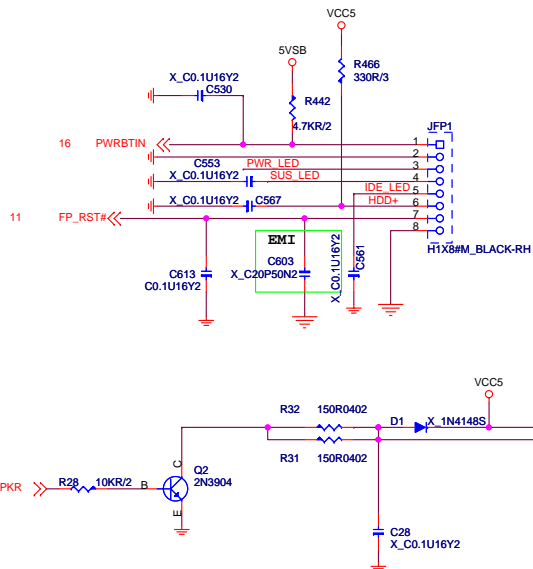


MICRO-STAR INT'L CO.,LTD		
MS-7502		
Size Custom	Document Description	Rev 1.1
VRD11-ISL6312 4-phase		
Date: Thursday, August 16, 2007	Sheet 27	of 33

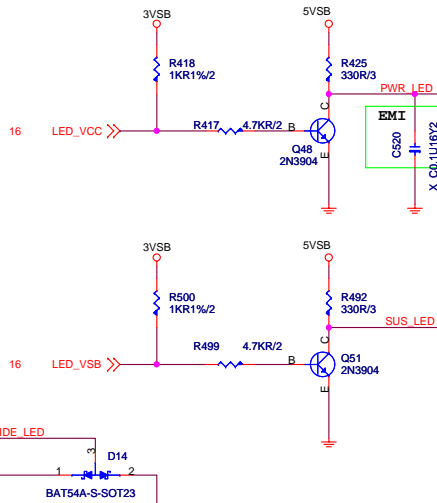
ATX POWER CONNECTOR



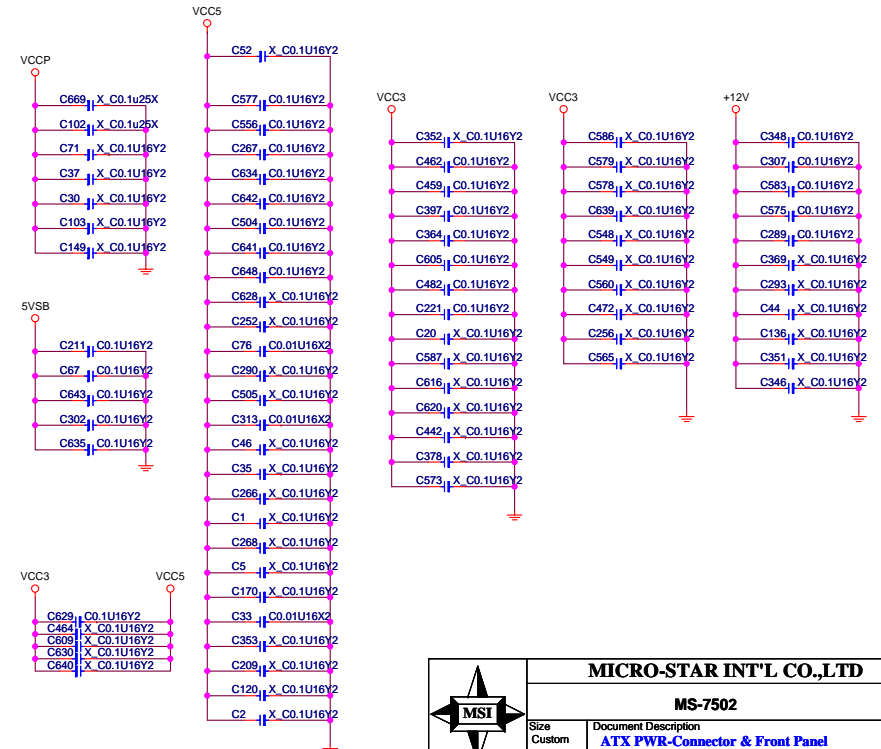
FRONT PANNEL



LED (for Fintek 71882)



Cap. for EMI & Power

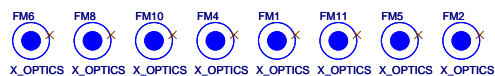


MICRO-STAR INT'L CO.,LTD		
MS-7502		
Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel	1.1
Date:	Thursday, August 16, 2007	Sheet 28 of 33

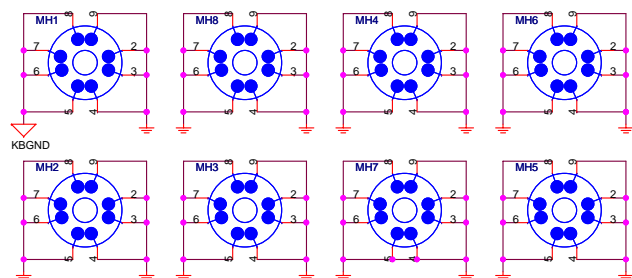
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



Simulation

